A1 cont. easily understood. Also, the numerical conditions explained below are merely examples to make the invention understandable."

Replace the paragraph beginning on page 8, line 8 with the following paragraph:

"When performing a functional test, the signal TEST supplied to the pad 106 is A2 set to the signal value for the functional test mode. As a result, the multiplexer 102 selects the pad 107, the multiplexer 103 selects the pad 108, the multiplexer 104 selects the signal Q, and the multiplexer 105 selects the clock CLK. Next, the test signal TD is input from the pad 107 and the test clock TCLK is input from the pad 108. The test signal TD and test clock TCLK are input to the macro cell 101 through the multiplexers 102 and 103. The macro cell 101 then reads the test signal TD at the time indicated by the test clock TCLK (rise time in the example in Figure 2), and outputs the signal Q of a value corresponding to the value of this test signal TD. This signal TQ is output from the pad 109 through the multiplexer 104. Also, the test clock TCLK is output as a clock MCLK from the pad 110 through the multiplexer 105."

Replace the paragraph beginning on page 8, line 23 with the following paragraph:

"In the present embodiment, the required time T1 from when the test clock TCLK A3 is supplied to the pad 108 until the pad 109 outputs the signal TQ and the required time

T2 from when the test clock TCLK is supplied to the pad 108 until the pad 110 outputs the test clock MCLK are measured. The difference between these required times T1-T2 is then calculated. As shown in Figure 2, when the time from when the test clock TCLK is applied to the pad 108 until the test clock TCLK is input to the macro cell 101 is t1; the time from when the macro cell receives the test clock TCLK until the macro cell outputs the signal Q (meaning access time) is tx; and the time from when the signal Q is output until this signal Q reaches the pad 109 is t2, then the time T1 = t1 + tx + t2. Also, as discussed above, the wiring delay from the output terminal Q to the pad 109 and wiring delay from the clock input terminal CLK to the pad 110 are substantially the same and therefore the time T2 = t1 + t2. Consequently, the time difference T1-T2 matches the access time tx. In other words, the time difference T1-T2 is the value obtained by removing the effect of the wiring delay from the measured value of the access time T1."

Replace the paragraph beginning on page 15, line 24 with the following paragraph:

"In the case of performing a functional test, the signal TEST supplied to the pad 408 is set at the signal value for the functional test mode. As a result, the multiplexer 404 selects the pad 409, the multiplexer 405 selects the pad 410, the multiplexer 406 selects the signal Q, and the multiplexer 407 selects the output signal of the latch 403. The test signal TD and test clock TCLK are input to the macro cell 401 through the

multiplexers 404 and 405. The macro cell 401 then outputs the signal Q. This signal TQ is output from the pad 412 through the multiplexer 406. Also, this signal Q is held in the latch 403. The signal Tq held in the latch 403 is output from the pad 411 through the multiplexer 407."

Replace the paragraph beginning on page 19, line 4 with the following paragraph:

"When performing a functional test, the signal TEST supplied to the pad 507 is set at a signal value for the functional test mode. Furthermore, the signal MODE supplied to the pad 506 is set at a signal value for selecting the signal input terminal D. As a result, the multiplexer 502 selects the pad 508, the multiplexer 503 selects the pad 509, the multiplexer 504 selects the signal Q, and the multiplexer 505 selects the signal input terminal D. The test signal TD is then input from the pad 508 and the test clock TCLK is input from the pad 509. At this time, after a prescribed period of time t1 from when the test signal TD is applied to the pad 508, the test clock TCLK rises and then after a prescribed period of time t2 from this rise time, the application of the test signal TD ends. These signals TD and TCLK are applied to the macro cell 501 through the multiplexers 502 and 503. The macro cell 501 receives the test signal TD at the rise time of the test clock TCLK and outputs the signal Q of a value corresponding to the value of this signal TD. This signal TQ is output from the pad 510 through the multiplexer 504. Also, the signal TD is output from the pad 511 through the multiplexer

a5 cont. 505. At this time, the required time T7, from when the test signal TD is supplied to the pad 508 until the pad 511 outputs the signal TD, is measured."

Replace the paragraph beginning on page 19, line 26 with the following paragraph:

a6 "Next, the signal MODE is converted to the signal value for selecting the clock input terminal CLK. At this time, the test clock TCLK is input from the pad 509. The test clock TCLK is output from the pad 511 through the multiplexers 503 and 505. The required time T8 from when the test clock TCLK is supplied to the pad 509 until the pad 511 outputs the test clock TCLK is measured."

In the Claims:

Please cancel claims 1-20 without prejudice or disclaimer of the subject matter contained therein.

Please add claims 21-42 as follows:

a7 --21. A semiconductor device having an access time measuring test mode, comprising:

a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal;